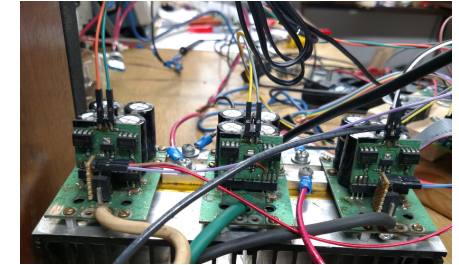


QFP100
PIN #s are
showing

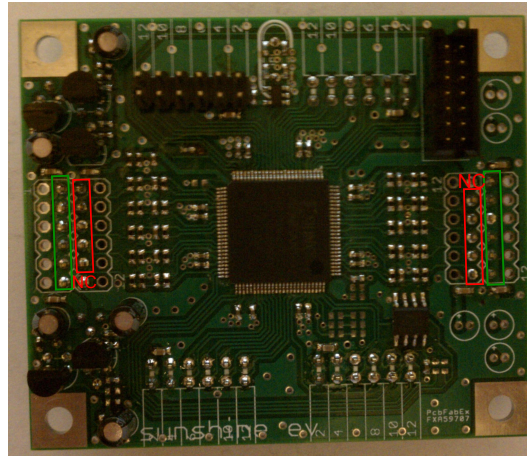
NC	NC	NC	NC	NC	RD
BRK_LIGHT	M1F_P	M2F_P	REVERSE_N	PMOD2_I_*	THROT
99	95	92	91	GND	PWR
98	94	NC	NC	GND	PWR
UART_TX	UART_RX	NC	NC	UART	RD_I_SENSE1/2
GY	WH	NC	NC	BK	RD

NC	WH	OR	YL	NC	NC
ANGLE2_IFB	M1AH	M1BH	M1CH	PMOD1_*	
89	86	84	79	GND	PWR
88	85	83	78	GND	PWR
ANGLE2_IFA	M1AL	M1BL	M1CL		
NC	BK	GN	GY	GN	NC

M1B	M1B	M1C	M1A
HIGH	OR	YL	WH
LOW	GN	GY	BK
PWR	RD		RD
GND	BR		BR
I_SENSE	PU		BL



GND	ADC	ADC_COMP_#	NEG	POS	DAC
GN	WH	GAS	0	3	2 4
NC	NC	BRK1_N	1	10	9 5
NC	NC	VALET_N	2	11	NC 12 CMOS
NC	NC	BRK2_N	3	16	5 17
NC	NC	BATT_I	4	23	22 18
NC	NC	NC			NC NC NC



NEG	POS	DAC #	ADC_COMP_#	ADC	GND
NC	NC	NC	NC	NC	NC
CMOS	71	NC	70	9	NEUTRAL_N
68	67	66	8	I2A	NC
63	62	65	7	I2B	NC
61	60	58	6	I1B	PU
54	53	57	5	I1A	BL

NC	NC	NC	NC	WH	NC
PMOD0_*	M2CL	M2BL	ANGLE1_IFA	M2AL	
PWR	GND	32	34	36	40
PWR	GND	33	35	38	41
PWR IN	M2CH	M2BH	ANGLE1_IFB	M2AH	
RD	BR	NC	NC	OR	NC

RD	BR	BL	BK	NC	NC
			M1	M2	
		SPI_CS2	SPI_CS1	SPI_CS0	INIT_B
PWR	GND	49	48	47	25
PWR	GND	50	44	27	26
RD	GY	NC	NC	NC	YL

used as chip select for SPI however this pin is "dout" which will be toggling during configuration.

